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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/679,658	10/04/2000	Moshe Gerstenhaber	AD-230J	8407

7590 06/17/2004

Iandiorio & Teska
260 Bear Hill Road
Waltham, MA 02451-1018

EXAMINER	
NGUYEN, DILINH P	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/679,658	GERSTENHABER ET AL.	
	Examin r	Art Unit	
	DiLinh Nguyen	2814	

-- The MAILING DATE of this communication appears on the cover sheet with th correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2000*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) *5-9* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election of embodiment 1 (figs. 3-4), claims 1-4 and 9-10 is acknowledged, but claims 9-10 disclose embodiment 2 (figs. 5-6). Therefore, claims 9-10 are withdrawn from the consideration.

Drawings

Figure 2 and 2A should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The drawings are objected to under 37 CFR 1.83(a) because they fail to show one of the output terminals and one of the power supply terminals are connected together and to a single pin as described in the claims 2 and 4. Any structural detail that is essential for a proper understanding of the disclosed invention should be shown in the drawing. MPEP § 608.02(d). A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Specification

The specification is objected to because they fail to show one of the output terminals and one of the power supply terminals are connected together and to a single pin as described in the claims 2 and 4.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 1) in view of Abedifard (U.S. Pat. 6445603).

- Regarding claims 1 and 3, AAPA discloses an integrated circuit chip package comprising:

a first and second power supply terminals V+ and V-; first and second input terminals –in and + in; first and second output terminals Vout and Vref; first and second gain resistor terminals RG; and a plurality of connection pins on the package for interconnecting with the terminals; and the input terminal – in is between the RG terminal and V- terminal (fig. 1, page 5, lines 15-23).

AAPA fails to disclose that first and second power supply terminals being connected to pins which are equally spaced from the pins to which the first and second gain resistor terminals are connected.

Abedifard discloses an integrated circuit chip package comprising: first power supply terminal Vcc and second power supply terminal Vss; wherein the first power supply terminal Vcc is located on one side of the integrated circuit chip package and the second power supply terminal Vss is located directly on an opposite side of the integrated circuit chip package (fig. 3, column 7, lines 15-17). Therefore, it would have

been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of AAPA (fig. 1) by having the first and second power supply terminals being connected to pins which are equally spaced from the pins to which the first and second gain resistor terminals are connected for balancing the effect of the package capacitance and reducing the common mode error with frequency with the structure as set forth above because as taught by Abedifard, such power supply terminals being connected to pin which are equally spaced would provide improvements in die efficiency (column 7, lines 47).

3. Claims 2 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (fig. 1) in view of Abedifard (U.S. Pat. 6445603) in view of Bowers (U.S. Pat. 5075633).

4. AAPA and Abedifard substantially discloses all the limitations as claimed above except one of the output terminals and one of the power supply terminals are connected together and to a single pin.

However, Bowers discloses a circuit comprising: one of the output terminals Vref and one of the power supply terminals V- are connected together and to a single pin (fig. 2, column 3, lines 14-16). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device structure of AAPA by having one of the output terminals and one of the power supply terminals are connected together and to a single pin with the structure as set forth above because as taught by Bowers, such single pin would balance the input to the circuit and allow for a symmetrical operation (column 3, lines 25-26).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to DiLinh Nguyen whose telephone number is (571) 272-1712. The examiner can normally be reached on 8:00AM - 6:00PM (M-F).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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